ST.ANNE'S

COLLEGE OF ENGINEERING AND TECHNOLOGY

(Approved by AICTE, New Delhi. Affiliated to Anna University, Chennai)
(An ISO 9001 **:** 2015 Certified Institution)
ANGUCHETTYPALAYAM, PANRUTI – 607 110.

QUESTION BANK

JULY 2018 - NOV 2018 / ODD SEMESTER

BRANCH: CSE **YR/SEM:** II/III **BATCH**: 2017 - 2021

SUB CODE/NAME: CS8351 – DIGITAL PRINCIPLES AND SYSTEM DESIGN

UNIT I

BOOLEAN ALGEBRA AND LOGIC GATES

PART A

1. Convert (101101.1101)2 to decimal and hexadecimal form.(MJ 2013)
2. What are the limitations of karnaugh map? (MJ 2013 &(ND 2017-R2013)
3. Find the octal equivalent of hexadecimal numbers of AB.CD.(MJ 2014-R2013)
4. State and prove the consensus theorem. (MJ 2014-R2013,MJ 2017-R2013 & ND 2016-R2013)
5. Convert (231.3)10 to binary. (MJ 2014-R2008)
6. Convert the binary number 10111011 into gray code. (MJ 2015-R2008)
7. What is mean by duality in Boolean algebra? (MJ 2015-R2008)
8. Convert (0.6875)10 to binary. (MJ 2015-R2013)
9. Prove the following using DeMorgan's Theorm. [(x+y)'+(x+y) '] '=x+y. (MJ 2015-R2013)
10. Find the octal equivalent of hexadecimal numbers of DC.BA. (MJ 2016-R2013)
11. What is meant by multilevel gates network? (MJ 2016-R2013)
12. Classify the logic families by its operations. (MJ 2017-R2013)
13. Write the truth table of AND and XOR gates. (ND 2010-R2008)
14. Perform the following code conversions: (ND 2011-R2008)

    (1010 .10)16 → (?)2→ (?)8 → (?)10 .
15. Convert $(1001010.1101001)_2$ to base 16 and $(231.07)_8$ to base 10. (ND 2013-R2008)
16. State the principle of duality. (ND 2014-R2013 & ND 2016-R2013)
17. Implement AND gate using only NOR gates. (ND 2014-R2013)
18. What is meant by self complementing code? (ND 2017-R2013)

19. Convert $(126)_{10}$ to Octal number and binary number. (ND 2015-R2013)
20. Write short notes on weighted binary codes. (ND 2015-R2013)

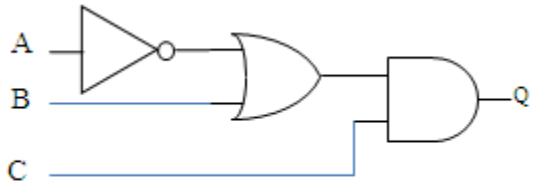
PART B

NUMBER SYSTEMS

1. Add, subtract and multiply the following numbers in binary 110010 and 11101.(6) (MJ 2014-R2008)
2. Convert (1947)10 into its equivalent octal and decimal representation (10) (ND 2010-R2008)
3. Perform (147-89) using 2's complement binary arithmetic. (6) (ND 2010-R2008)
4. Convert $(78.5)_{10}$ into binary.(3) (ND 2013-R2008).

LOGIC GATES

5. Convert the following logic system into NAND gates only.(8) MJ 2015-R2013)



6. Simplify the following expressions and implement them with two level NAND gate circuits: (16) (ND 2017-R2013)
   i. AB' +ABD+ ABD'+ A'C'D' +A'BC'
   ii. BD+BCD'+AB'C'D'
7. Implement the switching function f(x,y,z) = Σm(0,1,3,4,12,14,15) with NAND gates.(8) (ND 2016-R2013)

BOOLEAN EXPRESSION

8. Simplify the following expressions in (1) sum of the products and (2) products of sums :
   i) x'z' + y'z' + yz' + xy
   ii) AC'+B'D+A'CD+A'BCD
   iii) (A'+ B'+ D') (A + B'+ C') (A'+ B + D') (B + C'+ D') (16) (ND 2017-R2013)
9. Simplify the following Boolean function in Sum of Products (SOP) and (Product of Sums (POS) F(A,B,C,D) = Σm(0,1,2,5,8,9,10). (10) (ND 2014-R2013).
10. Express the following function in sum of min-terms and product of max-terms F(x,y,z)=x+yz. (8) (MJ 2015-R2013)
11. State and prove De Morgan's theorems (6/8) (ND 2010-R2008 & ND 2016-R2013)

KARNAUGH MAP METHOD

12. Reduce the following function using Karnaugh map technique: (16) *(MJ 2013)*
    i) f(A,B,C) = Σm(0,1,3,7) + Σd(2,5)
    ii) F(w,x,y,z) = Σm(0,7,8,9,10,12) + Σd(2,5,13)
13. Express the following function in a simplified manner using K map technique
    i. G=πM(0,1,3,7,9,11).
    ii. f(W,X,Y,Z)=Σm(0,7,8,9,10,12) + Σd(2,5,13).(16) (MJ 2013)
14. Simplify the following Boolean expression in
    (i) Sum of Product (8)
    (ii) Product of Sum using Karnaugh map.
    AC' + B'D + A'CD + ABCD. (16) MJ 2015-R2013)
15. Plot the following Boolean function in Karnaugh map and simplify it. F(w,x,y,z) = Σm(0,1,2,4,5,6,8,9,12,13,14). (6) (ND 2014-R2013).
16. Minimize the following expressions using K-Map
    Y= *A'BC'D' + A'BC'D + ABC'D' + A'B'CD'*. (10) (ND 2016-R2013)
17. Simplify the following switching functions using Karnaugh map method and realize expression using gates F(A,B,C,D) = Σ(0,3,5,7,8,9,10,12,15). (16) (ND 2015-R2013).

QUINE MCCLUSKEY OR TABULATION METHOD

18. Simplify the Boolean function using Quine McCluskey method.(16) *(MJ 2013)*
    F(A,B,C,D,E,F)= Σm(0,5,7,8,9,12,13,23,24,25,28,29,37,40,42,44,46,55,56,57,60,61).
19. Minimize the expression using Quine McCluskey(Tabulation) method.
    F=Σm(0,1,9,15,24,29,30) + Σd(8,11,31). (16) (MJ 2013)
20. Reduce the expression using Quine McCluskey method.
    F(x1,x2,x3,x4,x5)=Σm(0,2,4,5,6,7,8,10,14,17,18,21,29,31) + Σd(11,20,22). (16) (MJ 2016-R2013)
21. Minimize the following expressions using Quine McClusky method.
    Y= *A'BC'D' + A'BC'D + ABC'D' + ABC'D + AB'C'D +A'B'CD'.* (8) (ND 2016-R2013)
22. Simplify the function F(w,x,y,z) = Σ m(2,3,12,13,14,15) using tabulation method. Implement the simplified function using gates.(16) (ND 2014-R2013).
23. Simplify the following switching functions using Quine McClusky's method and realize expression using gates F(A,B,C,D) = Σ(0,5,7,8,9,10,11,14,15). (16) (ND 2015-R2013).
24. Simplify the following expression:
    $y = m_1+m_3+m_4+m_7+m_8+m_9+m_{10}+m_{11}+m_{12}+ m_{14}$ using
    (i) Karnaugh Map

(ii) Quine McClusky method. (16) (MJ 2017-R2013)

UNIT –II

COMBINATIONAL LOGIC

PART-A

1. Write down the truth table of a full subtractor. (MJ 2013-R2008 & ND 2017-R2013)
2. What is meant by Test Bench? (MJ 2013-R2008)
3. Implement the function G=Σm(0,3) using a 2x 4 deccoder. (MJ 2014-R2013)
4. Draw the circuit for 2 to 1 line multiplexer. (MJ 2014,ND 2016 & MJ 2017-R2013)
5. Realize G=AB'C+DE+F' using NAND gates. (MJ 2014-R2008)
6. Realise 4 bit binary to gray code converter using EX-OR gates. (MJ 2014-R2008)
7. Give the truth table for a half adder and write the expression for sum and carry. (MJ 2015-R2008)
8. Write any two advantages of HDL. (MJ 2015-R2008)
9. Implement a full adder with 4x1 Multiplexer. (MJ 2015-R2013)
10. Write the Data flow description of a 4-bit Comparator. (MJ 2015-R2013)
11. Define Combinational Circuits. (MJ 2016-R2013)
12. Design the combinational circuit with 3 inputs and 1 output. The output is 1 when the binary value of the inputs is less than 3.The output is 0 otherwise. (MJ 2016-R2013)
13. What is priority encoder. (MJ 2017 & ND 2016 - R2013)
14. With block diagram show how a full adder can be designed by using two half adders and one OR gate. (ND 2011-R2008)
15. Obtain the truth table for BCD to Excess-3 code converter. (ND 2013-R2008)
16. Define a code covereter logic circuit. (ND 2014-R2008)
17. What is half adder? Write its truth table. (ND 2014-R2008 & ND 2015-R2013)
18. Implement the following Boolean function using 8:1 multiplexer F(A,B,C)= Σm(1,3,5,6). (ND 2014-R2013)
19. What are binary decoders. (ND 2017-R2013)
20. Discuss NOR operation with truth table. (ND 2015-R2013)

PART-B

BINARY ADDER& SUBTRACTOR

1. Design a full adder With inputs x,y,x and two outputs S and C. The circuits performs x+y+z, z is the input carry, C is the output carry and S is the Sum.(16) (MJ 2016-R2013)

2. With neat diagram explain the 4-bit adder with carry lookahead.(8) (MJ 2015 & ND 2016-R2013)
3. Design a full subtractor with three inputs x and y and Bin and two outputs Diff and B_{out}. The circuit subtracts the bits x-y-Bin where Bin is the input borrow and diff is the difference. OR Design a full subtractor and derive expression for difference and borrow. Realize using gates. (16) (ND 2015-R2013)

MAGNITUDE COMPARATOR

4. Design 2-bit Magnitude Comparator and write a Verilog HDL code.(16) (ND 2014-R2013)

DECODERS – ENCODERS

5. Construct a 5 to 32 line decoder using 3 to 8 line decoders and 2 to 4 line decoder.(8) (MJ 2015-R2013)
6. Design a logic circuit that accepts a 4 bit grey code and converts it into 4 bit binary code. (16) (MJ 2016-R2013)
7. Design a code converter that converts a 8421 to BCD code. (16) (ND 2015-R2013)
8. Design a combinational circuit that converts 8421 BCD code to excess-3 code.(8/16) (ND 2016 & MJ 2014-R2013)
9. Design and implement binary to gray code convertor.(16) (ND 2017-R2013) & (ND 2014-R2008)
10. Design and implement a 8421 to gray code converter. Realize the converter using only NAND gates. (16) (ND 2014-R2013)
11. Compare and contrast between encoder and multiplexer.(8) (ND 2016-R2013)

MULTIPLEXERS

12. Implement the following Boolean function using 8 to 1 multiplexer F(A,B,C,D) = A'BD + ACD + B'CD + A'C'D. Also implement the function using 16 to 1 multiplexer. (16) (MJ 2014-R2013)
13. Implement the switching function F(A, B,C,D) = X (0, l, 3, 4,12,14,15) using 8 : 1 multiplexer. (ND 2017-R2013)
14. Implement the Boolean function using 8:1 multiplexer F(W,X,Y,Z)=W'XZ' +WYZ+ X'YZ+ W'Y'Z. (16) (MJ 2017-R2013)
15. Implement the following boolean function with a multiplexer: F(w,x,y,z) = Σ(2,3,5,6,11,14,15). (8) (MJ 2015-R2013)

HDL

16. Design a combinational circuit to convert binary to gray code.(16/8) (MJ 2013-R2008 & ND 2016-R2013)
17. Construct a BCD adder circuit and write a HDL program module for the same.(16) (MJ 2017-R2013)

UNIT –III

SYNCHRONOUS SEQUENTIAL LOGIC

PART-A

1. What is edge triggered flip flop? (ND 2017& MJ 2017)
2. How synchronous counters differs from asynchronous counters? (ND 2017)
3. What is the operation of JK flip flop? (ND 2016)
4. Define race around condition.(ND 2016 & MJ 2017)
5. Write notes on propagation delay. (ND 2015)
6. Draw the diagram of T flip flop and discuss it working. (ND 2015)
7. With reference to a JK flip flop, what is racing? (ND 2014)
8. Distinguish Moore and Mealy circuit.(ND 2014)
9. State the excitation table of JK flip flop. (MJ 2016)
10. What is the minimum number of flip flops needed to build a counter of modulus 8. (MJ 2016)
11. What is ring counter? (MJ 2015)
12. Give the block diagram of Master Slave D flip flop. (MJ 2015)
13. Write the characteristic table and equation of JK flip flop.(MJ 2014)
14. Write any two applications of Shift register.(MJ 2014)
15. Define shift register.(AM 2015-R2008)
16. Write the characteristic equation of a JK flip flop. (AM 2015-R2008)
17. Write down the characteristic equation of SR flip flop.
18. State the rules for state assignment.
19. What is the minimum number of flip flops needed to design a counter of modulus 60?
20. Compare combinational and sequential circuits.

PART-B

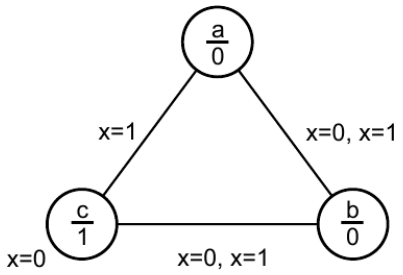
SEQUENTIAL CIRCUITS-FLIP FLOPS

1. Explain the operation of JK FF,SR FF, T FF and D FF with a neat diagram. Also discuss their characteristic equation and excitation table. (13) (ND 2017)
2. Implement JK flip flop using D flip flop.(8) (ND 2016)

3. How race condition can be avoided in a flip flop.(8) (ND 2016 & ND 2014)
4. Implement T flip flop and JK flip flop using D flip flop. (13) (MJ 2017) ***OR***
   Implement T flip flop using D flip flop and JK flip flop using D flip flop.(13) (MJ 2014)

ANALYSIS AND DESIGN OF CLOCKED SEQUENTIAL CIRCUITS

5. Realize the sequential circuit for the state diagram shown below.(8) (ND 2014)



6. A sequential circuit with two D flip flops A and B, one input x, and one output z is specified by the following next state and output equations:

   $A(t+1) = A' + B$,

   $B(t+1) = B' x$

   $z = A + B'$

   (i) Draw the logic diagram of the circuit.(4)

   (ii) Derive the state table.(3)

   (iii) Draw the state diagram of the circuit.(3) (MJ 2015)

7. Explain the differences between a state table, characteristic table and excitation table.(6) (MJ 2015)

COUNTERS

8. Design Mod-7 counter using JK flip flop. (13) (ND 2017)
9. Design a MOD-10 synchronous counter using JK flip flops.Write execution table and state table.(13) (ND 2014)
10. Design and implement Mod-5 synchronous counter using JK flip flop and also draw the timing diagram.(13) (MJ 2017)
11. Design a modulo 5 synchronous counter using JK Flip Flop and implement it .Construct its timing diagram.(14) (MJ 2016)
12. Consider the design of 4-bit BCD counter that counts in the following way: 0000,0001,0010….,1001 and back to 0000.Draw the logic diagram of this circuit.(14) (ND 2016)

13. Design a three bit synchronous counter with T flip flop and draw the diagram.(13) (ND 2015)
14. Design a binary counter using T flip flops to count in the following sequences: (14) (MJ 2016)
    i. 000,001,010,011,100,101,111,000
    ii. 000,100,111,010,011,000
15. Consider the design of a 4 bit BCD counter that counts in the following way: 0000,0001,0011…,1001 and back to 0000.
    (i) Draw the state diagram.(4)
    (ii) List the next state table.(4)
    (iii) Draw the logic diagram of the circuit.(8) (MJ 2015)
16. Deign a synchronous counter which counts in the sequence 000,001,010, 011,100,101, 110,111, 000 using D FF. (13) (MJ 2014)

UNIT- IV

ASYNCRONOUS SEQUENTIAL LOGIC

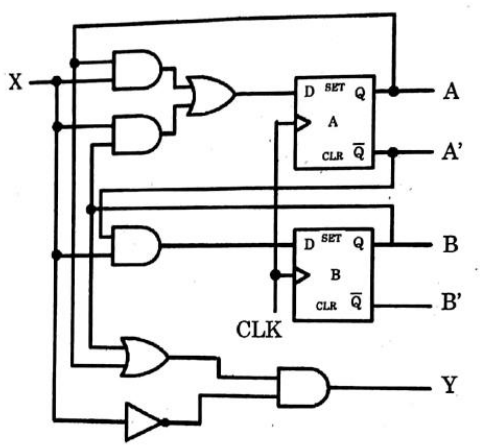
PART – A

1. What is asynchronous sequential circuit?
2. Define Merger graph. (ND 2017)
3. Define critical race and non critical race. (ND 2017 & MJ 2016)
4. What are races? (ND 2016)
5. Define flow table in asynchronous sequential circuits. (ND 2016)
6. What is race condition? (ND 2015 & MJ 2014)
7. Define Hazard. (ND 2014)
8. Define race around condition. (AM 2017)
9. Draw the waveforms showing static 1 hazard.(MJ 2016)
10. Compare synchronous and asynchronous sequential circuit.(MJ 2015)
11. What are the types of hazards? (MJ 2014)
12. What happens when hazard happens in a logic circuit?
13. What is meant by essential hazards?
14. Draw the block diagram of an asynchronous sequential circuit.
15. Define static hazard and dynamic hazard.
16. What is primitive flow table?
17. What are static 1 and static 0 hazards?

18. Define fundamental mode circuit and pulse mode circuit.
19. Write down the steps involved in the design of synchronous sequential circuits.
20. What is a critical race condition? Give example.
21. Compare synchronous and asynchronous sequential circuit.
22. What are hazard free digital circuits?
23. What are the types of asynchronous circuits?
24. Define flow table in asynchronous sequential circuit.
25. What is a critical race? Why should it be avoided?

PART - B

1. Explain about the designing of Asynchronous sequential circuits with example. (ND 2017) OR Explain the steps for design of asynchronous sequential circuits. (ND 2016 & MJ 2014) OR Summarize the design procedure of asynchronous sequential circuits. (AM 2017) (15)
2. What are Hazards and its types? How can you design a hazard free circuit, explain with example.(15) (ND 2017)
3. Explain the types of hazards in combinational circuits and sequential circuits and also demonstrate a hazard and its removal with example. (ND 2016 & MJ 2015) OR Explain the types of hazards that occurs in asynchronous sequential circuits and combinational circuits. (AM 2017) (15)
4. Discuss in detail the procedure for reducing the flow table with an example. (MJ 2016) (13)
5. Design an asynchronous sequential circuit with 2 inputs X and Y and with one output Z wherever Y is 1, input X is transferred to Z. When Y is 0; the output does not change for ant change in X. Use SR latch for implementation of the circuit. (15) (MJ 2016) (15)
6. Explain the race free assignment procedure .(8) (MJ 2015) OR Explain race free state assignment with a an example.(13)
7. Implement the switching function $F=\sum m(1,3,6,7,8,9,14,15)$ by astatic hazard free two level AND OR gate network. (15) (MJ 2014)
8. Analyze the following clocked sequential circuit and obtain the state equations and state diagram. (15) (ND 2015)



UNIT –V

MEMORY AND PROGRAMMABLE LOGIC

PART-A

1. What is memory decoding? (MJ 2014, ND 2017 & MJ 2017)
2. What is programmable logic array? How it differs from ROM? (ND 2017)
3. List the differences between PLA, PAL. (MJ 2017)
4. How to detect double error and correct single error? (ND 2016 & AM 2015)
5. Give the comparison between EPROM and PLA.(ND 2016)
6. What is memory address register?(ND 2015)
7. Write short notes PLA.(ND 2015)
8. Whether PAL is same as PAL? Explain.(ND 2014)
9. What is volatile memory? Give example. (ND 2014)
10. Define the critical rate and non critical rate. (MJ 2016)
11. Draw the wave forms showing static-1 hazard. (MJ 2016)
12. Differentiate between EEPROM and PROM.(AM 2015)
13. What is an implementation table? (AM 2015)
14. Write short notes on static-1 hazard. (AM 2015)
15. Define ASIC. (AM 2015)
16. Name the types of ROM. (AM 2011)
17. Compare and contrast static RAM and DRAM.(AM 2013)
18. Determine the number of address lines required for 512 bytes of memory and for a 2kB memory. (AM 2011)
19. Define a memory cell. Give an example. (AM 2007)
20. What is access time of a memory?

PART-B

RAM & ROM

1. Design a 16 bit RAM array (4 x 4 RAM) and explain the operation.(MJ 2017).(13)
2. Give the internal block diagram of 4x4 RAM. (6)
3. Design a combinational circuit using ROM that accepts a three bit binary number and outputs a binary number equal to the square of the input number.(13)
4. Discuss on the concept of working and applications of semiconductor memories.(13)

MEMORY DECODING

5. Write short notes on Address Multiplexing. (8)

ERROR DETECTION AND CORRECTION

6. Explain about error detection and correction using hamming codes. (13) (ND 2017)
7. The following messages have been coded in the even parity hamming code and transmitted through a noisy channel. Decode the messages assuming that at most a single error has occurred in each code word. i) 1001001 ii)0111001 iii)1110110 iv) 0011011. (15)

PLA

8. Explain in detail about Programmable Logic Array, Programmable Array Logic. (13) (ND 2017)
9. Implement the following using PLA: (13)

   $A(x,y,z) = \sum m(1,2,4,6)$

   $B(x,y,z) = \sum m(0,1,2,6,7)$

   $C(x,y,z) = \sum m(2,6)$

10. Draw a neat sketch showing implementation of Z1=ab`de` + a`b`c`e + bc + de, Z2=a`c`e, Z3=bc+de + c`de +bd and Z4=a`c`e + ce using a 5*8*4 PLA. (13)
11. Design a BCD to Excess-3 code converter and implement using suitable PLA.
12. Implement the following 2 Boolean functions with a PLA. (10)

    F1= AB` + AC + A`BC`

    F2=(AC +BC)`

PAL

13. Implement the following function using PAL $F1(A,B,C) = \sum(1,2,4,6)$, $F2=\sum(0,1,6,7)$, $F3(A,B,C)=\sum(1,2,3,5,7)$. (13)

SEQUENTIAL PROGRAMMABLE DEVICES

14. Briefly discuss the sequential programmable devices.(8)
15. Explain the following:

(i)	ASIC	(8)
(ii)	Field Programmable Gate Array	(8)